

IN THE CLAIMS

Please amend the claims as follows:

1. (canceled)

2. (canceled)

1 3. (currently amended) The VCO of claim [[2]]8, wherein the first PFET of the transfer
2 gate stage has a body terminal coupled to the first control voltage and the NFET of the
3 transfer gate a body terminal coupled to the second control voltage.

1 4. (currently amended) The VCO of claim [[1]]8, wherein the second control voltage is
2 derived from the first control voltage such that the first and the second control voltages
3 have a same nominal value and opposite slopes when modified.

1 5. (currently amended) The VCO of claim [[2]]8, wherein each of the CMOS inverters
2 in the K FF stages comprise a second PFET and a second NFET coupled in series,
3 wherein the second PFET of at least one of the CMOS inverters has a body terminal
4 coupled to the first control voltage and the second NFET of the at least one of the CMOS
5 inverters has a body terminal coupled to the second control voltage.

1 6. (original) The VCO of claim 3, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters
3 has a body terminal coupled to the first control voltage and the third NFET of the at least
4 one of the M CMOS inverters has a body terminal coupled to the second control voltage.

1 7. (original) The VCO of claim 5, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters
3 has a body terminal coupled to the first control voltage and the third NFET of the at least
4 one of the M CMOS inverters has a body terminal coupled to the second control voltage.

1 8. (currently amended) A voltage controlled oscillator (VCO) comprising a ring
2 oscillator having an input, an output, an odd number M of complementary metal oxide
3 semiconductor (CMOS) inverters series coupled between the input and output, a

4 feedback connection between the input and output, and a number K of voltage controlled
5 feed-forward (FF) stages, each of the K FF stages coupled in parallel with K groups of an
6 odd number of G sequential CMOS inverters selected from the M CMOS inverters, each
7 of the K FF stages having a plurality P channel metal oxide silicon transistors (PFETs)
8 and a plurality of N channel metal oxide silicon transistors (NFETs), at least one of the
9 PFETs having a first isolated region of semiconductor material (body) connected to a first
10 body terminal, and at least one of the NFETs having a second isolated body connected to
11 a second body terminal, wherein the K FF stages are controlled by first and second
12 control voltages coupled to the first and second body terminals respectively,

13 wherein each of the K FF stages comprises a CMOS inverter stage coupled in
14 series with a transfer gate stage having a parallel connection of a first PFET and a first
15 NFET, and ~~The VCO of claim 2,~~

16 wherein each of the CMOS inverters in the K FF stages comprise a second PFET
17 and a second NFET coupled in series, wherein the second PFET of at least one of the
18 CMOS inverters has a body terminal coupled to the first control voltage by a first
19 clamping circuit preventing a body diode coupled to the body terminal of the second
20 PFET from being forward biased and the second NFET of the at least one of the CMOS
21 inverters has a body terminal coupled to the second control voltage by a second clamping
22 circuit preventing a body diode coupled to the body terminal of the second NFET from
23 being forward biased.

1 9. (original) The VCO of claim 3, wherein each of M CMOS inverters comprise a
2 second PFET and a second NFET coupled in series, wherein the second PFET of at least
3 one of the CMOS inverters has a body terminal coupled to the first control voltage by a
4 first clamping circuit preventing a body diode coupled to the body terminal of the second
5 PFET from being forward biased and the second NFET of the at least one of the CMOS

6 inverters has a body terminal coupled to the second control voltage by a second clamping
7 circuit preventing a body diode coupled to the body terminal of the second NFET from
8 being forward biased.

1 10. (original) The VCO of claim 8, wherein the first clamping circuit comprises a
2 clamping PFET having a body terminal coupled to the source of the second PFET, a gate
3 coupled to ground potential, a drain coupled to the body terminal of the second PFET and
4 a source coupled to the first control voltage and the second clamping circuit comprises a
5 clamping NFET having a body terminal coupled to the source of the second NFET, a gate
6 coupled to the positive power supply voltage, a drain coupled to the body terminal of the
7 second NFET and a source coupled to the first control voltage.

1 11. (original) The VCO of claim 9, wherein the first clamping circuit comprises a
2 clamping PFET having a body terminal coupled to the source of the second PFET, a gate
3 coupled to ground potential, a drain coupled to the body terminal of the second PFET and
4 a source coupled to the first control voltage and the second clamping circuit comprises a
5 clamping NFET having a body terminal coupled to the source of the second NFET, a gate
6 coupled to the positive power supply voltage, a drain coupled to the body terminal of the
7 second NFET and a source coupled to the first control voltage.

1 12. (currently amended) The VCO of claim ~~[[1]]~~8, wherein K is equal to M.

13. (canceled)

14. (canceled)

1 15. (currently amended) The PLL circuit of claim ~~[[14]]~~20, wherein the first PFET of
2 the transfer gate stage has a body terminal coupled to the first control voltage and the
3 NFET of the transfer gate has a body terminal coupled to the second control voltage.

1 16. (currently amended) The PLL circuit of claim ~~[[13]]~~20, wherein the second control
2 voltage is derived from the first control voltage such that the first and the second control
3 voltages have a same nominal value and opposite slopes when modified.

1 17. (currently amended) The PLL circuit of claim ~~[[14]]~~20, wherein each of the CMOS
2 inverters in the K FF stages comprise a second PFET and a second NFET coupled in
3 series, wherein the second PFET of at least one of the CMOS inverters has a body
4 terminal coupled to the first control voltage and the second NFET of the at least one of
5 the CMOS inverters has a body terminal coupled to the second control voltage.

1 18. (original) The PLL circuit of claim 15, wherein each of M CMOS inverters
2 comprise a third PFET and a third NFET, wherein the third PFET of at least one of the M
3 CMOS inverters has a body terminal coupled to the first control voltage and the third
4 NFET of the at least one of the M CMOS inverters has a body terminal coupled to the
5 second control voltage.

1 19. (original) The PLL circuit of claim 17, wherein each of M CMOS inverters
2 comprises a third PFET and a third NFET, wherein the third PFET of at least one of the
3 M CMOS inverters has a body terminal coupled to the first control voltage and the third
4 NFET of the at least one of the M CMOS inverters has a body terminal coupled to the
5 second control voltage.

1 20. (currently amended) A phase locked loop (PLL) circuit for generating an output
2 clock signal with a frequency that is a multiple number N times the frequency of a
3 reference clock signal, comprising:

4 a voltage controlled oscillator (VCO) generating the output clock signal with a
5 frequency modified in response to a control voltage;

6 a frequency divider for frequency dividing the output clock signal by N,
7 generating a frequency divided clock signal;

8 a phase frequency detector for comparing the frequency divided clock signal to
9 the reference clock signal and generating a phase/frequency error signal; and

10 circuitry for converting the phase/frequency error signal to the control voltage, wherein
11 the VCO is a ring oscillator having an input, an output, an odd number M of
12 complementary metal oxide semiconductor (CMOS) inverters series coupled between the
13 input and output, a feedback connection between the input and output, and a number K of
14 voltage controlled feed-forward (FF) stages, each of the K FF stages coupled in parallel
15 with K groups of an odd number of G sequential CMOS inverters selected from the M
16 CMOS inverters, each of the K FF stages having a plurality P channel metal oxide silicon
17 transistors (PFETs) and a plurality of N channel metal oxide silicon transistors (NFETs),
18 at least one of the PFETs having a first isolated region of semiconductor material (body)
19 connected to a first body terminal, and at least one of the NFETs having a second isolated
20 body connected to a second body terminal, wherein the K FF stages are controlled by first
21 and second control voltages coupled to the first and second body terminals respectively,

22 wherein each of the K FF stages comprise a CMOS inverter stage coupled in
23 series with a transfer gate stage having a parallel connection of a first PFET and a first
24 NFET, and ~~The PLL circuit of claim 14,~~

25 wherein each of the CMOS inverters in the K FF stages comprise a second PFET
26 and a second NFET coupled in series, wherein the second PFET of at least one of the

CMOS inverters has a body terminal coupled to the first control voltage by a first clamping circuit preventing a body diode coupled to the body terminal of the second PFET from being forward biased and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage by a second clamping circuit preventing a body diode coupled to the body terminal of the second NFET from being forward biased.

21. (original) The PLL circuit of claim 15, wherein each of M CMOS inverters comprise a second PFET and a second NFET coupled in series, wherein the second PFET of at least one of the CMOS inverters has a body terminal coupled to the first control voltage by a first clamping circuit preventing a body diode coupled to the body terminal of the second PFET from being forward biased and the second NFET of the at least one of the CMOS inverters has a body terminal coupled to the second control voltage by a second clamping circuit preventing a body diode coupled to the body terminal of the second NFET from being forward biased.

22. (original) The PLL circuit of claim 20, wherein the first clamping circuit comprises a clamping PFET having a body terminal coupled to the source of the second PFET, a gate coupled to ground potential, a drain coupled to the body terminal of the second PFET and a source coupled to the first control voltage and the second clamping circuit comprises a clamping NFET having a body terminal coupled to the source of the second NFET, a gate coupled to the positive power supply voltage, a drain coupled to the body terminal of the second NFET and a source coupled to the first control voltage.

23. (original) The PLL circuit of claim 21, wherein the first clamping circuit comprises a clamping PFET having a body terminal coupled to the source of the second PFET, a gate coupled to ground potential, a drain coupled to the body terminal of the second PFET and a source coupled to the first control voltage and the second clamping circuit comprises a clamping NFET having a body terminal coupled to the source of the second

6 NFET, a gate coupled to the positive power supply voltage, a drain coupled to the body
7 terminal of the second NFET and a source coupled to the first control voltage.

1 24. (currently amended) The PLL circuit of claim ~~[[13]]~~20, wherein K is equal to M.

1 25. (new) A voltage controlled oscillator (VCO) comprising a ring oscillator having an
2 input, an output, an odd number M of complementary metal oxide semiconductor
3 (CMOS) inverters series coupled between the input and output, a feedback connection
4 between the input and output, and a number K of voltage controlled feed-forward (FF)
5 stages, each of the K FF stages coupled in parallel with K groups of an odd number of G
6 sequential CMOS inverters selected from the M CMOS inverters, each of the K FF stages
7 having a plurality P channel metal oxide silicon transistors (PFETs) and a plurality of N
8 channel metal oxide silicon transistors (NFETs), at least one of the PFETs having a first
9 isolated region of semiconductor material (body) connected to a first body terminal, and
10 at least one of the NFETs having a second isolated body connected to a second body
11 terminal, wherein the K FF stages are controlled by first and second control voltages
12 coupled to the first and second body terminals respectively,

13 wherein each of the K FF stages comprises a CMOS inverter stage coupled in
14 series with a transfer gate stage having a parallel connection of a first PFET and a first
15 NFET, and

16 wherein the first PFET of the transfer gate stage has a body terminal coupled to
17 the first control voltage and the NFET of the transfer gate a body terminal coupled to the
18 second control voltage.

1 26. (new) The VCO of claim 25, wherein the second control voltage is derived from the
2 first control voltage such that the first and the second control voltages have a same
3 nominal value and opposite slopes when modified.

1 27. (new) The VCO of claim 25 wherein each of the CMOS inverters in the K FF stages
2 comprise a second PFET and a second NFET coupled in series, wherein the second PFET
3 of at least one of the CMOS inverters has a body terminal coupled to the first control
4 voltage and the second NFET of the at least one of the CMOS inverters has a body
5 terminal coupled to the second control voltage.

1 28. (new) The VCO of claim 25, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters
3 has a body terminal coupled to the first control voltage and the third NFET of the at least
4 one of the M CMOS inverters has a body terminal coupled to the second control voltage.

1 29. (new) The VCO of claim 27, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters
3 has a body terminal coupled to the first control voltage and the third NFET of the at least
4 one of the M CMOS inverters has a body terminal coupled to the second control voltage.

1 30. (new) The VCO of claim 25, wherein each of the CMOS inverters in the K FF
2 stages comprise a second PFET and a second NFET coupled in series, wherein the
3 second PFET of at least one of the CMOS inverters has a body terminal coupled to the
4 first control voltage by a first clamping circuit preventing a body diode coupled to the
5 body terminal of the second PFET from being forward biased and the second NFET of
6 the at least one of the CMOS inverters has a body terminal coupled to the second control
7 voltage by a second clamping circuit preventing a body diode coupled to the body
8 terminal of the second NFET from being forward biased.

1 31. (new) The VCO of claim 25, wherein the first clamping circuit comprises a
2 clamping PFET having a body terminal coupled to the source of the second PFET, a gate
3 coupled to ground potential, a drain coupled to the body terminal of the second PFET and
4 a source coupled to the first control voltage and the second clamping circuit comprises a

5 clamping NFET having a body terminal coupled to the source of the second NFET, a gate
6 coupled to the positive power supply voltage, a drain coupled to the body terminal of the
7 second NFET and a source coupled to the first control voltage.

1 32. (new) The VCO of claim 25, wherein the first clamping circuit comprises a
2 clamping PFET having a body terminal coupled to the source of the second PFET, a gate
3 coupled to ground potential, a drain coupled to the body terminal of the second PFET and
4 a source coupled to the first control voltage and the second clamping circuit comprises a
5 clamping NFET having a body terminal coupled to the source of the second NFET, a gate
6 coupled to the positive power supply voltage, a drain coupled to the body terminal of the
7 second NFET and a source coupled to the first control voltage.

1 33. (new) The VCO of claim 25, wherein K is equal to M.

1 34. (new) A phase locked loop (PLL) circuit for generating an output clock signal with a
2 frequency that is a multiple number N times the frequency of a reference clock signal,
3 comprising:

4 a voltage controlled oscillator (VCO) generating the output clock signal with a
5 frequency modified in response to a control voltage;

6 a frequency divider for frequency dividing the output clock signal by N,
7 generating a frequency divided clock signal;

8 a phase frequency detector for comparing the frequency divided clock signal to
9 the reference clock signal and generating a phase/frequency error signal; and

10 circuitry for converting the phase/frequency error signal to the control voltage, the
11 VCO is configured as a ring oscillator having an input, an output, an odd number M of
12 complementary metal oxide semiconductor (CMOS) inverters series coupled between the
13 input and output, a feedback connection between the input and output, and a number K of
14 voltage controlled feed-forward (FF) stages, each of the K FF stages coupled in parallel

15 with K groups of an odd number of G sequential CMOS inverters selected from the M
16 CMOS inverters, each of the K FF stages having a plurality P channel metal oxide silicon
17 transistors (PFETs) and a plurality of N channel metal oxide silicon transistors (NFETs),
18 at least one of the PFETs having a first isolated region of semiconductor material (body)
19 connected to a first body terminal, and at least one of the NFETs having a second isolated
20 body connected to a second body terminal, wherein the K FF stages are controlled by first
21 and second control voltages coupled to the first and second body terminals respectively,

22 wherein each of the K FF stages comprise a CMOS inverter stage coupled in
23 series with a transfer gate stage having a parallel connection of a first PFET and a first
24 NFET,

25 wherein the first PFET of the transfer gate stage has a body terminal coupled to
26 the first control voltage and the NFET of the transfer gate has a body terminal coupled to
27 the second control voltage, and

28 wherein each of the CMOS inverters in the K FF stages comprise a second PFET
29 and a second NFET coupled in series, wherein the second PFET of at least one of the
30 CMOS inverters has a body terminal coupled to the first control voltage by a first
31 clamping circuit preventing a body diode coupled to the body terminal of the second
32 PFET from being forward biased and the second NFET of the at least one of the CMOS
33 inverters has a body terminal coupled to the second control voltage by a second clamping
34 circuit preventing a body diode coupled to the body terminal of the second NFET from
35 being forward biased

1 35. (new) The PLL of claim 34, wherein the second control voltage is derived from the
2 first control voltage such that the first and the second control voltages have a same
3 nominal value and opposite slopes when modified.

1 36. (new) The PLL of claim 34 wherein each of the CMOS inverters in the K FF stages
2 comprise a second PFET and a second NFET coupled in series, wherein the second PFET
3 of at least one of the CMOS inverters has a body terminal coupled to the first control
4 voltage and the second NFET of the at least one of the CMOS inverters has a body
5 terminal coupled to the second control voltage.

1 37. (new) The PLL of claim 34, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters
3 has a body terminal coupled to the first control voltage and the third NFET of the at least
4 one of the M CMOS inverters has a body terminal coupled to the second control voltage.

1 38. (new) The PLL of claim 36, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS inverters
3 has a body terminal coupled to the first control voltage and the third NFET of the at least
4 one of the M CMOS inverters has a body terminal coupled to the second control voltage.

1 39. (new) The PLL of claim 34, wherein each of the CMOS inverters in the K FF stages
2 comprise a second PFET and a second NFET coupled in series, wherein the second PFET
3 of at least one of the CMOS inverters has a body terminal coupled to the first control
4 voltage by a first clamping circuit preventing a body diode coupled to the body terminal
5 of the second PFET from being forward biased and the second NFET of the at least one
6 of the CMOS inverters has a body terminal coupled to the second control voltage by a
7 second clamping circuit preventing a body diode coupled to the body terminal of the
8 second NFET from being forward biased.

1 40. (new) The PLL of claim 34, wherein each of M CMOS inverters comprise a second
2 PFET and a second NFET coupled in series, wherein the second PFET of at least one of
3 the CMOS inverters has a body terminal coupled to the first control voltage by a first
4 clamping circuit preventing a body diode coupled to the body terminal of the second

5 PFET from being forward biased and the second NFET of the at least one of the CMOS
6 inverters has a body terminal coupled to the second control voltage by a second clamping
7 circuit preventing a body diode coupled to the body terminal of the second NFET from
8 being forward biased.

1 41. (new) The PLL of claim 39, wherein the first clamping circuit comprises a clamping
2 PFET having a body terminal coupled to the source of the second PFET, a gate coupled
3 to ground potential, a drain coupled to the body terminal of the second PFET and a
4 source coupled to the first control voltage and the second clamping circuit comprises a
5 clamping NFET having a body terminal coupled to the source of the second NFET, a gate
6 coupled to the positive power supply voltage, a drain coupled to the body terminal of the
7 second NFET and a source coupled to the first control voltage.

1 42. (new) The PLL of claim 34, wherein the first clamping circuit comprises a clamping
2 PFET having a body terminal coupled to the source of the second PFET, a gate coupled
3 to ground potential, a drain coupled to the body terminal of the second PFET and a
4 source coupled to the first control voltage and the second clamping circuit comprises a
5 clamping NFET having a body terminal coupled to the source of the second NFET, a gate
6 coupled to the positive power supply voltage, a drain coupled to the body terminal of the
7 second NFET and a source coupled to the first control voltage.

1 43. (new) The PLL of claim 34, wherein K is equal to M.